

ABSTRACT OF DISCLOSURE

A fraction part control circuit of a frequency synthesizer apparatus including a PLL circuit is of a plural-n-th-order delta-sigma modulator circuit for controlling a fraction part of a number of frequency division to a variable frequency divider of the PLL circuit. An adder adds data of the fraction part to an output data from a multiplier and outputs the resultant data to a quantizer through a second-order integrator. The quantizer quantizes input data with a quantization step and outputs the quantized data to the multiplier through a feedback circuit. The quantized data is used as data of the controlled fraction part. The multiplier multiplies data from the feedback circuit by the quantization step and outputs the resultant data to the adder. The fraction part control circuit periodically changes the data of the fraction part, thereby setting a frequency of an output signal from a VCO according to an average value of the period.